A copy of the marked up amended specification and claims are attached to this response showing the changes as set forth in 37 C.F.R. § 1.121.

REMARKS

Claims 1-20 are pending in this application, wherein claims 12-18 are withdrawn from consideration and claims 19-20 are added. By this Amendment, claims 1 and 8 are amended to recite "being in a stage after metal wiring is formed". Support for the amended and added claims is found in the specification. No new matter is added.

This reply is submitted as a complete and full response to the outstanding Office Action. Reconsideration of the application in view of the above amendments and following remarks is respectfully requested.

MATTERS OF FORM

The Office Action rejects claims 3-5 and 7-8 under 35 U.S.C. § 112, second paragraph, asserting lack of antecedent basis. Applicants have amended the claims to obviate this rejection. Accordingly, Applicants respectfully request the withdrawal of this rejection.

CLAIMS 1-11 UNDER 35 U.S.C. § 103(a)

The Office Action rejects claims 1-11 under 35 U.S.C. § 103(a) over the Applicants' prior art (APA) in view of Fudanuki et al. (U.S. Patent No. 6,054,872, hereinafter as "Fudanuki"). This rejection is respectfully traversed.

Applicants' independent claim 1 recites a fundamental cell, used as a basic unit in layout of a semiconductor integrated circuit device and being in a stage after metal wiring is formed, comprising, no fixed wiring for commonly wiring between fundamental cells, and connector terminals to be connected to upper wiring layers.

Applicants' independent claim 8 recites a semiconductor integrated circuit device, comprising, a fundamental cell, used as a basic unit in layout and being in a stage after metal wiring is formed, having no fixed wiring to be commonly wired between the basic units, and having connector terminals to be connected to upper wiring layers, and upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental cell.

The features described in the Applicants' claimed invention enable a fundamental cell's structure wherein there is no commonly fixed wiring between the fundamental cells.

As admitted in the Office Action, the APA does not disclose "no fixed wiring for commonly wiring between fundamental cells". However, the Office Action asserts that Fudanuki supplies the subject matter lacking in the APA. Applicants respectfully disagree for the reasons set forth below.

Fudanuki shows an integrated circuit wherein a plurality of standard cells are arranged and fundamental cells of gate arrays are arranged on open regions. Though, Fig. 10A of Fudanuki shows the "arrangement" of the fundamental cells without wiring among the fundamental cells, Fig. 10B demonstrates the equivalent metal wirings that are necessary for the fundamental cells of Fig. 10A to operate. See, for example, col. 12, lines 42-67.

Similarly, Fig. 5B of Fudanuki shows fixed wirings (e.g., power rails) VDD 9 and VSS 10 arranged between the fundamental cells. That is, Fig. 5B shows the entirety of the chip on which the metal wirings are arranged.

Therefore, as demonstrated in Figs. 10B and 5B of Fudanuki, Fudanuki requires the fixed wirings to be arranged between fundamental cells. See col. 12, lines 45-50 and col. 9, lines 42-44, for example.

In contrast, as recited in Applicants' independent claims, "no fixed wiring or commonly wiring between fundamental cells". Thus, it is readily apparent that Fudanuki does not supply the subject matter lacking in the APA. Therefore, the APA and Fudanaki, individually or in combination, do not disclose or suggest all the claimed features of Applicants' invention.

Claims 2-7 depend from claim 1 and claims 9-11 depend from claim 8. Accordingly, for at least the above reasons, Applicants respectfully request the withdrawal of this rejection.

The Office Action rejects claims 1-11 under 35 U.S.C. § 103(a) over Yuyama et al. (U.S. Patent No. 5,117,277, hereinafter as "Yuyama"), and Fudanuki. This rejection is respectfully traversed.

As admitted in the Office Action, Yuyama does not disclose "no fixed wiring for commonly wiring between fundamental cells". However, the Office Action asserts that Fudanuki supplies the subject matter lacking in Yuyama. For at least the same reasons discussed above, Applicants respectfully submit that Fudanuki does not disclose or suggest the subject matter lacking in Yuyama.

For example, Fudanuki's embodiments disclose the use of designated areas for placement of high potential power supply wirings (VDD) 11 and the lower potential power supply wirings (VSS) 12 placed along boundaries between upper cell rows and

lower cell rows. See col. 12, lines 45-50, for example. Thus, it is readily apparent that Fudanuki does not supply the subject matter lacking in Yuyama.

In view of the above, Applicants respectfully submit that Yuyama and Fudanaki, individually or in combination, do not disclose or suggest all the claimed subject matter of Applicants' invention.

Claims 2-7 depend from claim 1 and claims 9-11 depend from claim 8. Thus, for at least the above reasons, Applicants respectfully request the withdrawal of this rejection.

CONCLUSION

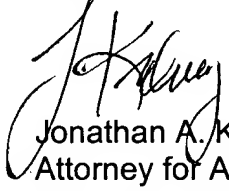
In view of the above remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance of claims is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge

payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 024016-00014.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosures: Marked-Up Copy of Amended Specification
Marked-Up Copy of Amended Claims
Petition for Extension of Time (one month)

MARKED-UP COPY OF AMENDED SPECIFICATION

Page 1, paragraph 2, beginning at line 15:

A semiconductor integrated circuit device of the gate array type and standard cell type is used so far, in which functional circuit blocks constituted of fundamental cells in a matrix structure are arranged. Fig. 12 shows a typical example of a fundamental cell 100. The fundamental cell 100 has therein a power supply voltage wiring VDD and ground potential wiring VSS, or so-called the power rails VDD and VSS in order to supply the power supply voltage VDD and [grand] ground potential VSS respectively to the fundamental cell 100. Connection terminals 2 and 3 are used for biasing N-type well region of a PMOS (P-channel metal oxide semiconductor) transistor and a P-type well region of an NMOS (N-channel metal oxide semiconductor) transistor to the power supply voltage VDD and the ground potential VSS, respectively.

MARKED-UP COPY OF AMENDED CLAIMS

1. (Once Amended) A fundamental cell, used as a basic unit in layout of a semiconductor integrated circuit device and being in a stage after metal wiring is formed, comprising:

no fixed wiring for commonly wiring between fundamental cells [each other], and

[connection] connector terminals to be connected to upper wiring layers.

8. (Once Amended) A semiconductor integrated circuit device, comprising:

a fundamental cell, used as a basic unit in layout and being in a stage after metal wiring is formed, having no fixed wiring to be commonly wired between the basic units, and having connector terminals to be connected to upper wiring layers; and

upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental [cells] cell.